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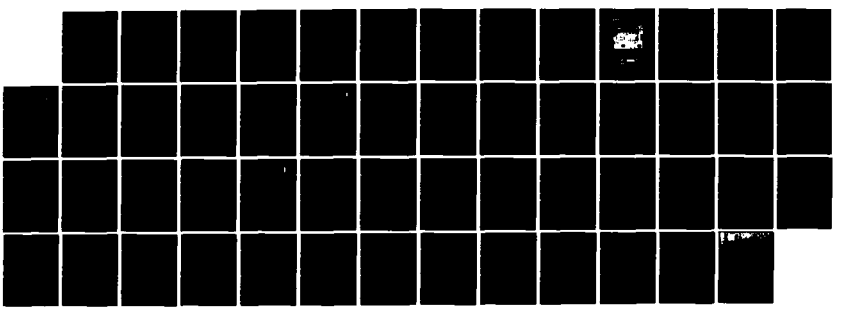

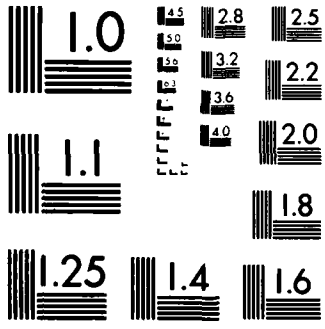

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SWITCHABLE 10-BIT PCM DECODER

R. F. BUCK

Electronics Laboratory - C.E.A.T.
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This report describes a portable, self-contained switchable 8-channel 10-bit PCM decoder, designed as a complementary item of dedicated test equipment for use in checkout and qualification testing of airborne PCM encoders, constructed for use in the "falling sphere" class of atmospheric density experiments. The system provides 8 channels of analog output data, suitable for use in stripchart recording. Six of these channels are switchable to any desired digital word within the data stream; one switchable channel is additionally provided with a 10-bit binary display for the digital data in the selected word. A second switchable

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Block 20. ABSTRACT (Continued)

channel also permits decommutation of subcommutated housekeeping data within word 15 of the PCM data. A parallel digital data output is provided to allow interface with automated testing equipment for qualification testing.

The report also provides detailed data concerning the computer-controlled automatic temperature qualification test procedure used in certifying the airborne apparatus for flight, including the step-by-step routine to be followed in performing the tests.

SUMMARY

The OSU Model C90TD11 PCM decoder has been developed for convenience in checkout and qualification testing of the continuing series of Model C40BE01B airborne PCM encoders constructed under AFGL contract, for installation in "falling sphere" instruments used to measure atmospheric density and wind structure.

The decoder is a small self-contained item of ground support equipment which may be used for bench test and checkout, or for field support applications during rocket launch activities. It provides panel readout (in digital or analog form) of the data from the decoder. A total of eight outputs in analog form, suitable for use with conventional strip-chart recorders, are available. Two channels are permanently dedicated to words 13 and 14 of the normal format, while five others may be switched to any desired word within the minor data frame. A sixth switchable channel may be used either for decoding subcommutated housekeeping data within word 15, or for a selected word from 8 to 15 within the minor frame.

A parallel data interface connector permits use with the computer-controlled automatic temperature qualification test equipment used in final testing, in order to provide hard-copy documentation of test results.

The report covers design details, theory of operation, and test procedures. In addition, an updated description of the automated test set-up is included; an appendix covers the computer software used in performing the automated test.

PREFACE

The work reported herein was sponsored by the Aerospace Instrumentation Division of the Air Force Geophysics Laboratory, Hanscom Air Force Base, Massachusetts, under DOD contract F19628-81-C-0079.

Gratitude is expressed to the Contract Manager, Jack R. Griffin/LCR, Sounding Rocket Branch, for encouragement and support of the development and construction of the apparatus described.

Additional appreciation is expressed to J. W. Spears and Philip L. Parsons for their contributions in the development of the automated test equipment and computer software utilized in the performance of the automatic qualification test routines.

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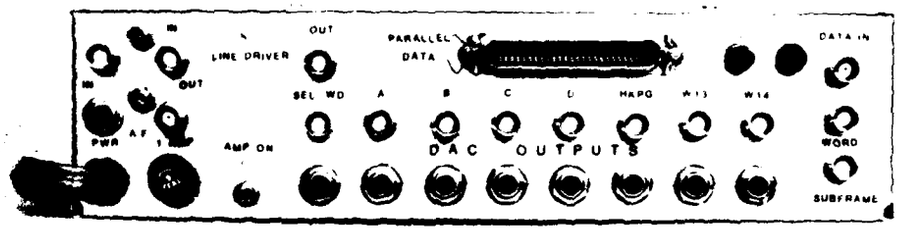
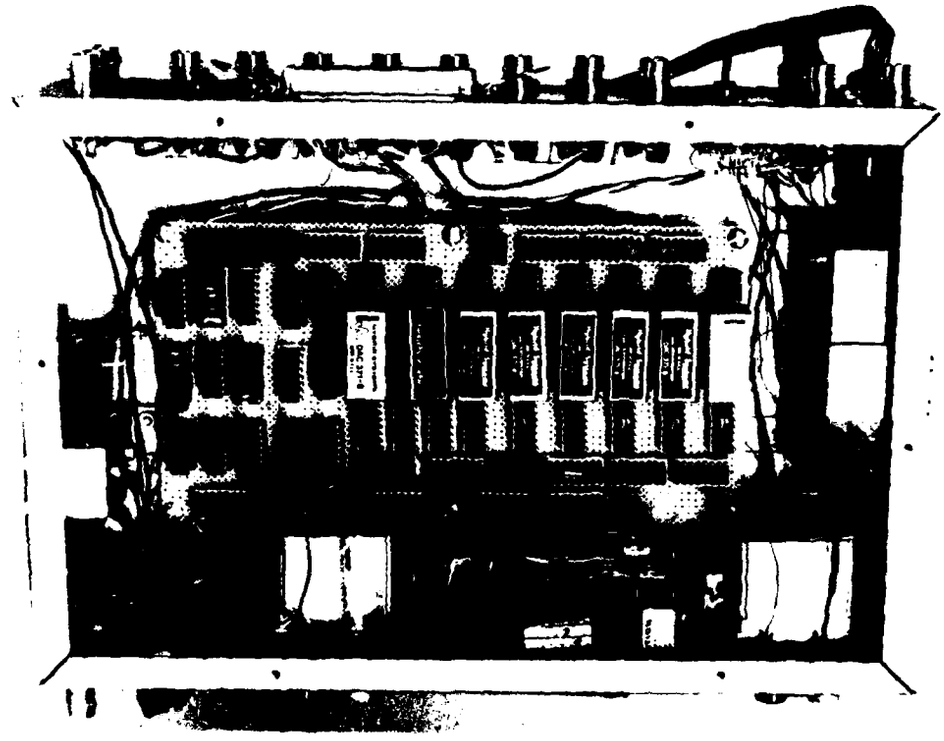


Rear Panel



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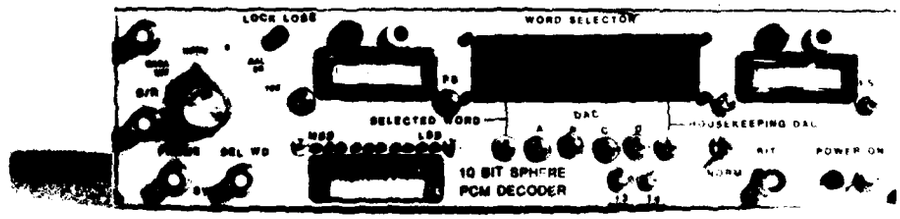

Front Panel

Switchable 10-Bit PCM Decoder

SWITCHABLE 10-BIT PCM DECODER
(Test of Falling Sphere Encoder)

1.0 INTRODUCTION

1.1 The OSU model C90TD12 switchable 8-Channel 10-bit PCM decoder was developed for test and checkout of the 10-bit airborne encoders, constructed for use in the Accumetrics falling sphere instrument. The model C40BE01 encoder, developed for this purpose, has been described previously (Reference 1). The decoder was developed as a portable self-contained instrument, capable of facilitating bench tests of the encoders when built and interfacing with the automated PCM encoder temperature test equipment constructed by OSU for temperature test qualification of completed encoders. It is also usable for field support, in decoding the incoming telemetry from the sphere instrument and providing suitable analog outputs for strip-chart recorder.

1.2 Characteristics of the PCM signal to be decoded are as follows: 20 Kilobit per second Biphase-Level coded data, most significant bit first, with a word length of 10 bits and a minor frame of 16 words. Subcommutation is provided through an 8-frame subcom, available in the word 15 position. Minor frame synchronization is in the form of the standard 10-bit Barker code (110 111 000 0), inserted in the "word 0" position, with alternate frames inverted to the binary complement of the Barker code. No subframe ID is provided; subframe synchronization in the "frame 0" position is provided by a subframe synchronization word of ten consecutive 0's. Normal data input span is bipolar, from -5.00 volts (all "0" code) to +5.00 volts (all "1" code). Subframe data input range is restricted to the positive end of this range (0 volts = 100 000 000 0, +5 volts = 111 111 111 1).

1.3 Previous test equipment developed for this same purpose included a special test set, designed to permit operation of the encoder independent of the instrument and to facilitate initial test and setup of the encoder analog-to-digital converter. Details of this test box and its proper use have been described previously (Reference 1 Section 4.0). As an auxiliary aid to use of this falling sphere [illegible], a special dedicated "all-words" PCM decoder, complementing the airborne sphere encoder, was also constructed, and has been previously described (Reference 2, Section 8.4). The model reported herein was based on a somewhat simplified version of the original "all-words" decoder,

repackaged into a size which can conveniently be carried in an ordinary brief case or attache case (3"x8"x12", exclusive of connectors).

1.4 Special features incorporated into this new piece of apparatus are as follows:

(a) Six switchable analog equivalent outputs, capable of driving an associated strip chart recorder with 0 to +5 volt drive at 12 milliampere maximum current, together with two additional analog outputs with similar characteristics, permanently wired to words 13 and 14. (This provides a capability of driving the standard 6-channel Brush recorder. If an 8-channel recorder is available, it permits addition of the commonly monitored word 13 (nutation output) and word 14 (Supply voltage monitor) from the associated instrument.)

(b) One of the selected outputs is provided with both a 10-bit digital binary light display and an analog monitor signal, adjustable for conversion of the binary digital data to the normal analog equivalent voltage of 0 to 5.00 volts full scale. In addition, a second one of the switchable outputs is so wired as to permit its use with either selected main words within the stream, or for subcommutation of the housekeeping data in word 15. (This system is restricted to 8-bit digital-to-analog conversion, but does include an adjustable analog monitor signal of the decoded subcommutation data.)

(c) Circuitry is also provided internal to the decoder to permit interface directly with the OSU computer-controlled automated temperature test apparatus (Reference 3). A standard 50-pin parallel data output connector is available, which provides both ten-line parallel data from the decoder, and binary-coded-decimal two-digit word address information.

(d) As a convenience for field operation, the system has also been provided with an accessory line driver, with BNC input and output connections and a gain control, to permit its use to drive external apparatus through a long coaxial cable, terminated to minimize reflection. In addition, a microphone preamplifier has also been provided internal to the unit, with standard Littleplug 12B input connector and BNC output, also with adjustable level. (This is for convenience in adding audio to the associated tape recorder when using the device under field conditions.) The decoder also provides a monitor of the Biphase-Level signal input and the NRZ-Level output data from the shift register internal to the unit, as well as synchronizing signals at bit rate, word rate, frame rate, and subframe rate, all automatically derived within the unit.

2.0 SIMPLIFIED THEORY OF OPERATION (Refer to Block Diagram B90TD11, Figure 1)

2.1 Incoming data from PCM system (either directly from the encoder under test, or from the associated telemetry ground station in flight) is brought into the unit through the Op/Cal switch to a data conditioner, which serves to standardize the PCM biphase data to the desired 0 to +5 volt logic level, squared and shaped for proper operation in following circuitry. A transition detector within the data conditioner is used to generate clocking by detecting the mid-bit transistion present in the biphase level signal and using it to trigger a bit clock multi-vibrator, IC108, which provides timing to the remainder of the unit. Bit clock pulses are counted down 10 to 1 in IC109, to provide an output at word rate. This clock is then counted down to the 16 consecutive words which constitute 1 frame by word counter IC110. Reset pulses at frame rate from the word counter are also combined with the subframe synchronizing signal and used to operate a frame counter, IC121, counting down by a factor of 8 to the major frame frequency.

2.2 Conditioned data is fed through a sync inversion gate, whose operation will be described later, as serial data input to a 20-bit shift register, using IC115/116/117. Inversion of alternate frames of the synchronizing signal prior to entry in the shift register insures that all data within the shift register is in "normalized" form. This data is clocked through by the bit clock signal from IC108A and continuously provides two consecutive words of data from the incoming stream, for use within the remainder of the unit.

2.3 The shift register, at the time of synchronization, contains word 15 of one frame and word 0 of the next following frame. Ten bits of the shift register then contain the main frame synchronizing signal code, and the other ten bits hold the pattern present in word 15 from the preceding frame. A frame synchronizing detector, IC118/119, detects the proper pattern of 1's and 0's and, as the last bit of the synchronizing word enters the shift register, provides an output frame synchronizing signal, which is used to trigger a blanking flip-flop IC111, generating a frame reset pulse to bit counter, word counter, and frame counter, as well as to the word address generator portion of the circuit. During the frame synchronizing pulse which immediately follows the subframe synchronization pattern of all 0's, a similar subframe sync detector has 10 consecutive 0's clocked in, and thus gates the detected subframe sync with the main frame sync, to provide an output signal for the subcommutation portion of the decoder.

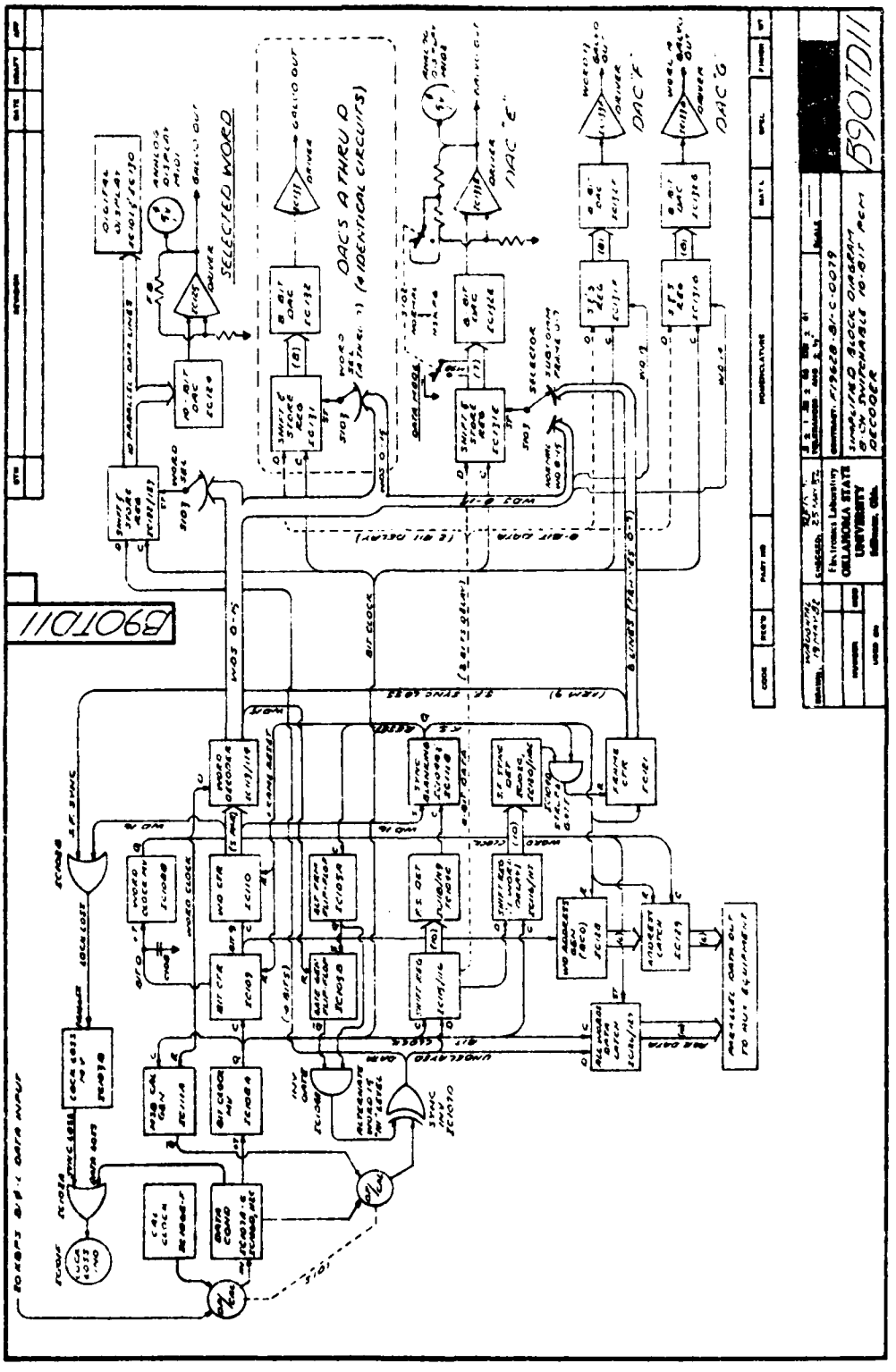

Figure 1. Block Diagram, Decoder

2.4 Inversion of the alternate incoming synchronization signal is accomplished by counting down consecutive frame sync reset pulses in the flip-flop, IC105A. The Q output from this flip-flop is used to set gate generator flip-flop IC105B, which is then reset by the "word 15" signal from the word decoder. The $\bar{Q}$ output of the gate generator flip-flop is then combined with alternate frames from IC105A by inversion gate IC104A and used to control one input signal to exclusive or gate IC107D. The net effect is that the sync inverter gate IC107D operates as a normal buffer amplifier for all data words and for every other frame synchronizing word; during word 15 of every other frame, this chip becomes an inverter, thus restoring the "normal" synchronizing wave pattern.

2.5 The bit-clock multivibrator signal from IC108A is counted down by a factor of 10 in bit counter IC109. The output signal is used to trigger word counter IC110 and word address generator IC128; the reset bit signal from the same decade counter is used to trigger a word clock multivibrator, IC108D. The word clock is derived from the output signal of this multivibrator. This word clock signal is then used in the remainder of the circuit for clocking purposes. Word counter IC110 provides address lines to the word decoder, IC113/114, which provides a sequence of sixteen word outputs on separate lines for words 0 through 15, used in timing all of the digital-to-analog converter circuits which follow. In a similar manner, "reset signals" from the sync blanking flip-flop are used as frame clock input to a frame counter/decoder, IC121, which is reset by the detected subframe synchronization. This decoder then provides a sequence of eight output lines for frames 0 through 7, for use as timing for the subcommutation portion of the circuit.

2.6 Operation of the "Selected Word" digital-to-analog conversion portion of the circuit typifies the philosophy used throughout the decoder. Undelayed 10-bit data from shift register input line is clocked into shift-and-store register, IC122/123, by the bit clock line and then strobed into latch form by the "selected word" gate pulse. This is selected by S103, one section of a hexadecimal switch, permitting selection of words 0 through 15. The shift register output is then latched in ten-line parallel output form at the output of the shift-and-store register. The 10-bit pattern is provided as a visual digital display by IC101 and IC130, driving an array of 10 LED indicators on the front panel. Simultaneously, the 10 parallel data lines are fed as parallel input to a 10-bit digital-to-analog converter, IC124. The analog equivalent of this digital word is used as input to IC125, an operational amplifier provided

with gain and zero adjust controls, so as to scale the output properly to a 0 to +5 volt analog voltage form. This signal is displayed on analog meter M101, and also is taken through an attenuator pot to a jack on the rear, where it may be used to drive an associated galvanometer.

2.7 Channels "A" though "D" of the decoder operate in exactly the same form, but operate from an input data line which is delayed two bits in order to use the most significant 8 bits for the associated 8-bit DAC. (The data is clocked through with a 2-bit delay to insure the right 8 bits are in place, and then strobed into position by the selected word gate from additional sections A through D of hexadecimal switch S103.) The 8-line parallel output is then converted to analog form and fed through a simple operational amplifier to an associated galvanometer output. No analog or digital display is provided for these four circuits.

2.8 The "E" channel of the decoder is provided with two modes of operation: it can operate either in the "normal" data mode for selected main frame word 8 through 15, or in a "housekeeping" mode in which the operation is on one selected frame of word 15, through position 0 through 7 of the section S103E of the hexadecimal switch. In the "normal" data mode, operation is exactly as described above; in the "housekeeping mode", subcommutation input is used and the strobe pulse is derived from a selected frame from the frame counter. Toggle switch S102 selects either "normal" or "housekeeping" mode. In the housekeeping mode, the first bit of the 8-bit signal is grounded and the scale factor for associated amplifier IC133E is adjusted by changing the feedback resistor. By this means, the most significant bit of the signal, which serves only to indicate that the data is of positive polarity, is deleted from the conversion process and the amplifier gain is increased by a factor of 2, so that the 0 to 5 volts analog output range corresponds to a true 0 to 5 volt "housekeeping data" input range. This channel is also provided with an analog display meter, as well as the galvanometer output.

2.9 Two additional digital-to-analog converter channels are provided, but are not switchable. These sections of the decoder provide an analog equivalent of words 13 and 14, and are hardwired to the word decoder lines for word 13 and 14. The 8-bit delayed data is again strobed into position at the time of the two desired words, converted to analog form, and fed through an operational amplifier to an attenuator, permitting adjustment of each associated galvanometer.

2.10 As an indication to the operator that PCM data is being entered and properly decoded, the decoder is provided with a "lock-loss indicator". This panel-mounted LED, IC101F, can be illuminated by any of the following conditions: loss of data, loss of frame synchronization, or loss of subframe synchronization. (In the loss of subframe synchronization, the "lock-loss" light will blink; loss of data or frame synchronization will provide steady illumination of the light.) Operation is as follows:

(a) In the event there is no data input to the decoder, IC107C in the data conditioner circuit will detect the fact that a PCM wavetrain is not present. This will then send a DC signal through "or" gate IC102A, illuminating the lock-loss indicator through IC101F, the lamp driver.

(b) In the event frame synchronization is lost, word counter IC110 will not be reset by a detected frame synchronizing pulse. A signal from the word counter will then be fed through the "or" gate, IC102B, as a trigger to the lock-loss multivibrator, IC103B. The multivibrator time constant is set so the period is such that the output which occurs at each failure to detect frame synchronization is adequately long to feed through gate IC102A to the lock-loss indicator, thus causing it to glow, even if the "data loss" line is not high.

(c) When operating in the "housekeeping" subcommutation mode, an output from the frame counter IC121 is also generated if S.F. synch is lost. This is coupled through IC102B and triggers the lock loss multivibrator. This will also generate a multivibrator pulse sufficiently long to illuminate the "lock-loss" indicator. However, the low frequency of the subframe synchronization signal is such that the light will visually flicker under these conditions, indicating that the loss is in the subframe synchronization only. (In the event the decoder is operated in the "normal" mode without subcommutation capability, this portion of the circuit is disabled.)

Note that, if in the calibration mode, the data loss line will not be energized, since it will be driven by the cal clock generator. However, the fact that there is no frame synchronizing word in the cal mode will cause the "lock-loss" light to come on, indicating that the system operation is abnormal when in the "calibrate" mode.

2.11 As a convenience to the operator in adjusting the scale factor for "Selected Word" and "E" channel outputs to the desired scale factor, and also assist in setting up the associated analog strip-chart recorders, this system

has been provided with an internal calibration generator, which will permit generation of digital words corresponding to 0, 50%, and 100% full scale for the associated DAC. In this mode of operation, clocking for the system is provided by an internal oscillator, IC106E/F, which generates a free-run clock signal at approximately normal bit rate, to be clocked through the data conditioner. Input to the shift register is grounded for the "0" calibration position, providing a sequence of 10 consecutive 0's. For the "50%" cal mode, IC111A is reset by the word clock line and the $\bar{Q}$ output taken to the input of the shift register. Since data is clocked through by the bit clock line, this generates a sequence of a 1, followed by nine 0's. For the "100%" calibration mode, the shift register input is strapped to +5 volts, and the clock then runs through a continuous sequence of 1's, generating the full-scale calibration voltage.

2.12 In order to facilitate use of this decoder with the automated test routine, the portion of the circuit shown at the lower left of the block diagram has been added. Undelayed 10-bit data is clocked into the all words data latch, IC126/127 by the bit clock signal. This data is latched into position once per word by the work clock line from IC108B. The 10-bits of parallel data output are then taken to a parallel data out connector for connection to auxiliary equipment. Word clock pulses from the trailing edge of bit 9 of the bit counter chain are used as clocking pulses to the word address generator, IC128. This counter is reset by detected frame synchronizing pulses, thus establishing a 0 point for the word address count. IC128 generates standard 4-bit BCD coded lines for "units" and the first two digits of the "tens" count, and provides these as input signals to the address latch chip, IC129. This address is latched into place by the word clock line and reset by the frame sync line to insure that, simultaneously with presentation of the data in parallel form, the address of the word being displayed is also available on six additional output lines to the auxiliary equipment. Since the latching function is performed by the word clock, this data is updated once per word and thus provides all words in parallel-line form, together with each associated word address signal.

3.0 DETAILED THEORY OF OPERATION (Reference Schematic Diagram C90TD12, Figure 2)

3.1 Incoming PCM data is taken through either the "INV" or "NORM" position of the data/cal swith S101A and capacity coupled to one input of exclusive or gate IC107A. The second input to this gate is grounded. DC bias to the input

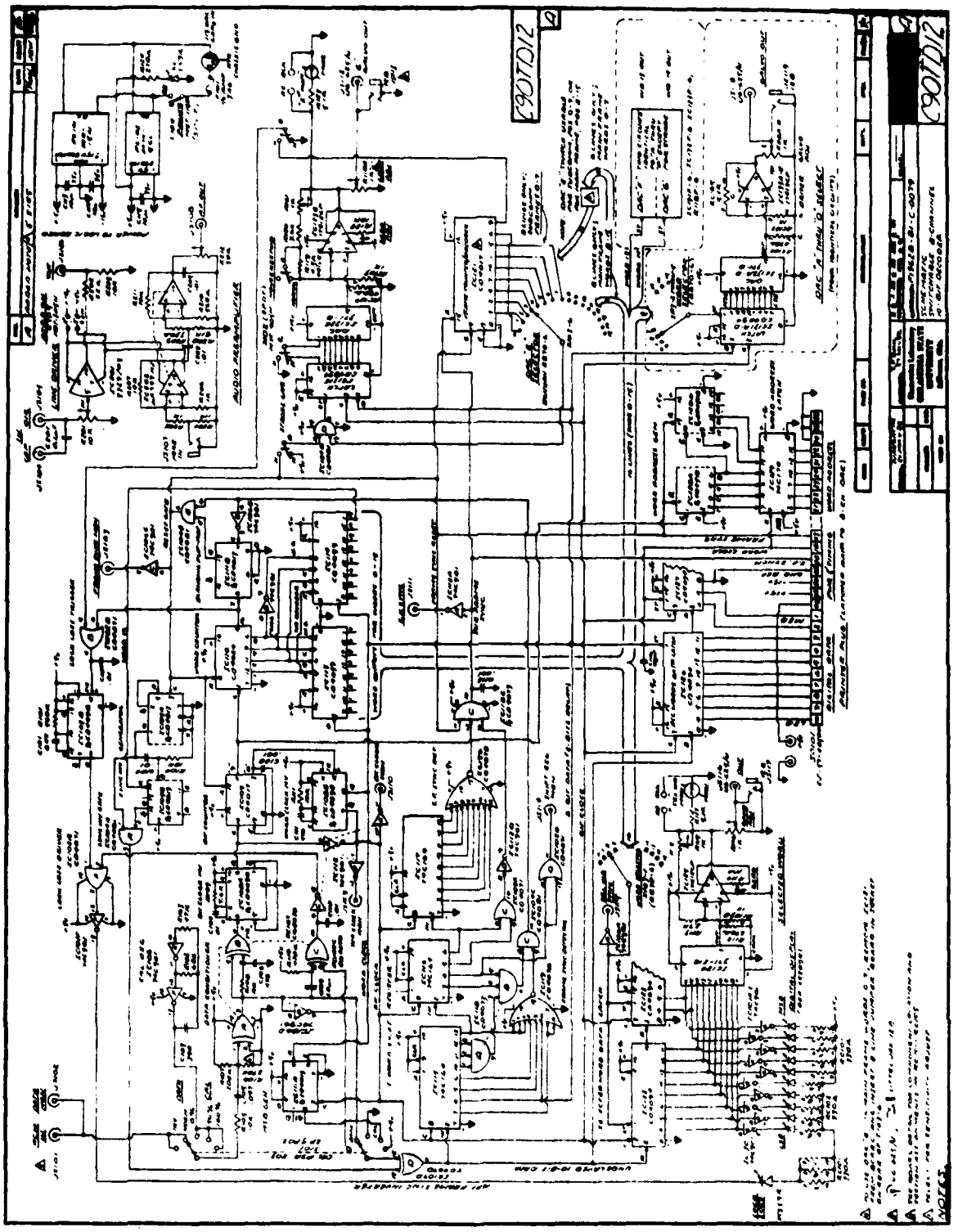

Figure 2. Schematic Diagram, Decoder

to which the signal is applied is adjusted by selecting resistors R106 and R107, so as to keep the threshold just below the trip point. Capacity-coupled transitions then will drive the pin 1 input positive during incoming "1" signals, and negative during "0" levels. By proper adjustment of R106, it is possible to set the threshold of this chip to a value of approximately 0.2 volts peak-to-peak for the incoming wave train; it will function properly on signal levels of ±10 volts as well. R105 limits input to the chip under high drive conditions. This insures that the data conditioner operates at any usable input signal level. The action of IC107A is to slice a narrow portion from the incoming waveform, providing standardized "0" and "5 volt" logic levels at its output, pin 3. The standardized and shaped biphase level signal from pin 3 is taken directly to the "NORMAL" position of a second section of the data/cal switch S101B; the same signal is inverted by IC106D and taken to the "INV" position of the same switch. PCM data from FM discriminators of either polarity may be used for following portions of the system.

The same conditioned signal is then taken directly to pin 5 of IC107B, a second exclusive-or gate. The signal is also delayed slightly by a filter network (R108 and C106 in series) and applied to the pin 6 input. This section of the chip then functions as a transition detector because of the slight delay between the input signal to pins 5 and 6. The net effect is that spikes are generated at the output (pin 4) for each transition of the input bilevel signal. These detected positive transitions are then used to trigger the bit clock multivibrator, IC108A. This is a normal one-shot multivibrator with a time constant so chosen as to generate, from each trigger, an output signal at pin 6 which is approximately 3/4 bit in width. Note that, because this is slightly larger than the half-bit time period of the incoming wavetrain, the system will "lock on" to the mid-bit transition because a 1-0 or 0-1 transition in the data line will be effectively two half-bits in width, thus forcing the clock to lock on to the desired mid-bit transition. This signal, taken directly from the Q output on pin 6, serves as the $\overline{\text{clock}}$ signal to advance bit counter IC 109, a decade divider chip, at the mid-bit transition of each bit of the incoming data stream. The $\overline{\text{clock}}$ signal is inverted to a true bit clock line by IC112B and used as the "bit clock" signal to the remainder of the decoder. (Note that the asymmetry of the bit clock multivibrator serves to accomplish approximately a one-quarter bit phase shift in the sense of the clocking by means of this scheme, and it is constantly referenced to the

mid-bit transition, which is always present in a biphase level signal.) The bit clock line is also reinverted by IC112E and brought to a BNC jack on the panel as a bit clock monitor.

Conditioned data from the arm of data/cal switch S101B is taken through the sync inverter gate, IC107D, to provide the undelayed 10-bit data line for the shift registers IC115-IC117 and data latches IC122/123 and IC126/127, where undelayed 10-bit data is desired. A 20-bit shift register is made up from IC115/116/117, and the 10-bit conditioned data is clocked through this register by the bit clock line described previously. The timing clock described previously provides that data at the pin 2 entry point to the shift register chain will always be clocked in approximately one-quarter bit later, allowing settling time prior to entry to the shift registers.

3.2 The bit clock is counted down to work clock frequency by bit counter IC109, a divide-by-10 counter. The output from the "9" count is used as input to the word counter chain because IC110 operates on the negative-going transition; the negative-going transition of the "9" output is effectively in synchronization with the positive-going transition of the "0" count, which is used to trigger word clock multivibrator, IC108B. The narrow positive-going output of the one-shot multivibrator (from the Q output of pin 10) is used as the word clock signal for the remainder of the unit. The $\bar{Q}$ output on pin 9 is taken through IC112F, inverted to the normal clock form, and provided as a word clock monitor on a BNC jack on the decoder, for external use. IC110, the word counter, is a conventional binary counter operating on input clock signals from the bit counter and providing parallel 1, 2, 4, 8, and 16 coded output lines. Under normal conditions, the word counter will be reset by the detected and gated frame sync pulse, insuring that an output at the pin 5 "16" output is never high more than the momentary transient which occurs at the time of reset. However, if a frame synchronizing pulse is not detected after 16 words, this signal will go high and operate the "lock-loss" signal in the manner to be described later. The 1, 2, 4, and 8 line outputs are used as address lines to the word decoder chain. (The 8 line is also inverted by IC106D and used to enable the second half of the word decoder chain.)

3.3 The desired Barker code frame synchronizing pulse in the "word 0" position is detected by wiring the 10 parallel outputs of the first 10 bits of the shift register to a pattern detector. The and gates of IC118A and B serve to detect "1" bits in position 1, 2, 4, 5, and 6, providing a positive-

going signal at pin 6 of IC118B. IC119 simultaneously detects the presence of 0's in the third bit and bits 7 through 10. The combined outputs of IC118B and IC119 are then summed in and gate IC104C so as to provide a detected sync pulse when all 10 bits are in the proper position in the register; this pulse is used for the reset gate and to drive the sync blanking flip-flop.

A type D flip-flop, IC111B, is normally set with the Q high by the output pulse from pin 5 of word counter IC110, enabling the reset gate, IC104B. Immediately thereafter, when frame sync is detected, the output of the frame sync detector is used to clock this flip-flop through inverter gate IC106B. Simultaneously, the positive-going sync pulse goes through gate IC104B and serves as the "reset" line to the remainder of the decoder. This gated frame sync reset pulse is inverted by IC106C and made available as a frame sync monitor on the panel. The "reset" line is also used as the frame synchronizing signal to the remainder of the decoder, where it is used to reset word counters and bit counters, as well as the word address generators. This pulse, occurring only at the time of the start of "word 1" (end of "word 0") is also used to advance the frame counter/decoder, IC121, another decade counter decoder chip which will be used for a frame counter and detector in the subcommutation decoding operation, to be described later.

3.4 The incoming data stream has alternate frame synchronizing words inverted to the binary complement of the normal Barker code word. In order to stay synchronized with this alternating sequence of frame synchronizing words, an automatic method of frame sync reinversion is required. The inversion is supplied by exclusive or gate IC107D at the input to the shift register, operating on the digital data line at pin 12 of this chip. Input to pin 13 for this gate is normally held in a low state, but is automatically driven high during every other "word 0". In order to generate the desired inversion gate, the detected frame sync "reset" gate from IC104B is used to trigger flip-flop IC105A, which alternates states with each successive frame sync pulse. The Q output from pin 1 is taken as one input to inverting gate generator IC104A, and also capacity-coupled to IC105B, a set/reset flip-flop, which is thus set with the Q high and the $\bar{Q}$ low at the time of frame sync. The "word 15" decoded output from IC114 is then brought in as a "reset" pulse to this same flip-flop, resetting the Q low and driving the $\bar{Q}$ output high at the beginning of word 15. (This synchronization is normal for the unit.) $\bar{Q}$ will then be set low again by the next following positive transition from

IC105A. The net result is a positive gate at pin 3 of IC104A, starting at the beginning of "word 15" and ending at the beginning of "word 0" once every other frame. Timing is such that this inverting gate occurs one frame behind the normal detected frame sync pulse, and thus the next following frame period will provide the necessary one-word-wide gate to IC107D, inverting the Biphase-Level data stream only during the alternate "word 0" periods of the synchronizing signal. The net result is that the undelayed 10-bit data line from IC107D has all synchronizing words re-established in the normal Barker code bit pattern; this data is clocked through the shift register and also used as the data line for the remainder of the decoder.

3.5 Chips IC113/114 provide a 16-word decoder chain with parallel address inputs in binary form, derived from word counter IC110, which clocks through the "word clock" line such that a positive gate, 600 Microseconds wide, is steered through the register, which is reset by the frame synchronizing pulse. The decoder provides a narrow positive gate on each of the 16 lines in sequence, as timing proceeds through the main frame. Sixteen output lines from this signal are taken to the 16 inputs of each section of S103, a 6-section hexadecimal switch. The 16 positions of these switches are marked as words 0 through 15, and permit selecting the desired signal for strobing data into each of the latches elsewhere in the system. Note that any of the 6 switchable units can be manually selected for any desired word, including word 0, the sync word.

3.6 For subcommutation detection, it is also necessary to determine synchronization for word 15, in which the subcommutated data lies. The synchronizing word pattern generated within the coder is a sequence of ten 0's; the other 10 bits of the 20-bit shift register are used for subframe sync detection, and the first 8 bits are taken to a multiple nor gate, IC120. Bits 9 and 10 are taken through or gate IC102C and then inverted by IC112D, effectively providing a second nor gate for the last two bits. At the time when all 10 bits are simultaneously at 0, these two signals are fed to pins 12 and 13 of chip IC118C, a triple-input and gate. The third input to this gate is derived from the frame sync "reset" line. (Note that, because the 20-bit shift register effectively provides a 1 word delay between the first 10 bits and the second 10 bits, all 20 bits for subframe sync and main frame sync will be in position simultaneously (with subframe sync in word 15 and frame sync in word 0) at the time an output pulse is generated at pin 10 of IC118C, providing

subframe synchronization.) This signal is taken through inverter chip IC112A to a subframe sync test jack on the decoder. It also is provided on the parallel data output plug SO101, and is used as the reset pulse to the frame counter decoder, IC121. IC121 is advanced by the normal minor frame sync "reset" line and thus, in a manner similar to that previously described for the word decoder, provides a frame decoder. It is reset to major frame sync reference by the detected subframe sync, and advances on each following minor frame sync, to generate output gate pulses at minor frame rate through the entire major frame sequence of frames 0 through 7. These eight enable lines are taken to the "E" section of the hexadecimal switch and wired to position 0 through 7, such as to permit selection of any frame within the subcommutation sequence from which data is desired through the subcom decoder. Note that normally, if the system remains in synchronization, the "reset" pulse will restore the count to zero before an advance can be made to the equivalent "frame 8" position; if a frame sync is lost and the counter advances beyond this point, an output signal is generated which can be used in the "lock-loss" trigger section to indicate loss of subframe sync.

3.7 Selection of a desired word, latching parallel data into the data register, and conversion to analog form are performed automatically for each of the eight possible sections of the decoder. Full operation is provided by the left-hand word selector switch, which permits selection of words 0 through 15 as strobe lines to a 10-bit data latch. This latch is made up of IC122 and part of IC123. Undelayed 10-bit data is fed to this latch and clocked through by the bit clock. At the time of the selected word, the positive going gate, selected by S103, is fed in as a strobe light, freezing the 10 output lines into the parallel representation of the bit pattern. Each of these 10 lines then operates through a lamp driver (IC101A through E, and IC130A through E) so as to drive an LED lamp on the front panel. Each lamp is provided with a 330 ohm series resistor, (RC101 and 102) to current limit lamp current. Any output lines high result in illuminating the lamp; low lines leave the light extinguished, thus presenting 1's as illuminated and 0's as dark in the binary digital display. The same 10 input lines are also fed into a 10-bit DAC, IC124, where they are detected and summed in a resistance ladder to develop an output voltage proportional to the decimal value of binary-coded input signal. This voltage, developed across resistor R112, is then taken through IC125, an operational amplifier, so wired as to have adjustable feedback through R115 to

pin 2 for adjustment of "full-scale" gain, and an offset "zero" trim adjustment by means of R114 for balancing. The output signal from pin 6 of the operational amplifier is taken to a 0 to 5 volt analog volt meter, M101, and also to a pair of jacks on the front panel; the same signal is divided by R116, an attenuator pot, and taken to a pair of output jacks on the rear panel, where it can be used either for BNC or phone jack connections to an associated recording meter, with adjustable deflection. Note that this operational amplifier is provided with both zero and full-scale adjustments, allowing the system to be set-up for all 0's (to represent 0 volt) and all 1's (to represent 5 volts), to provide an external digital presentation of the value of the input word by means of a DVM. The selected word gate from the arm of switch S-103-1 is also taken through an inverter, IC106A, as a "selected word sync" pulse to a BNC jack which can be used for synchronization of an external scope, if desired. By this means, scope sync can be varied for each word in the format to provide an expanded presentation of the digital data corresponding to any given word.

3.8 The next four sections of switch S103 correspond to A, B, C, and D DAC outputs. Each can be individually selected for the desired word, and they function in the same general manner just described for the selected word. DAC's with only 8-bit resolution are used in these channels, and therefore it is necessary to delay the digital input by 2 bits, in order to decode the 8 most significant bits of each word at the desired time. (This is accomplished by driving the data latches for these channels by a signal tapped 2 bits into the data register, deriving the 8-bit input data signal from pin 4 of IC115.) Data is clocked into the latch in serial form by the bit clock and strobed into the latched position by the selected word from S103, as described previously. After conversion to analog form, the signal is again run through galvo drivers (IC133 A through D) and provided as an adjustable analog output on the rear panel. No monitor point or digital display is provided for these DAC's.

3.9 The conversion and decoding for the "E" channel of this system is somewhat different. This channel can be used in either the "Normal" mode, where it is capable of selecting mainframe words 8 through 15, or in the "Housekeeping" mode, where it is capable of detecting word 15 subcommutated data from frames 0 through 7. S103-6 permits selection of the desired timing for the strobe signal, and IC104D provides the strobe gate to the associated latch, IC131E. A two-position toggle switch, S102, is provided to permit use of this channel in either the "Normal" (bipolar 5 volt data words, 8 through 15)

or "Housekeeping" (word 15, selected frame 0 through 7, with 0 to +5v limit on data input and 0 to 5v data span output). For the subcom mode of operation, this switch should be thrown to the "Housekeeping" position. In this mode of operation, strobe gate IC104D combines the frame synch "reset" line with a selected frame gate, to generate the strobe signal to latch IC131E. Note that, because data is delayed one word in the shift register, this is equivalent to latching in the data at the end of the selected word fifteen. The same "Housekeeping" position of this switch also disables the most significant bit for the DAC input, by grounding one input to the 371-8 DAC and thus providing 7-bit conversion, equivalent to a signal from band center to upper-band edge. A third section of this switch doubles the gain for the operational amplifier by changing feedback under these conditions of operation, and a fourth section of S102 enables the subframe sync loss portion of the "lock-loss" detector.

In the "Normal" mode of operation, strobe gate IC104D is enabled by +5 volts, and thus gates in selected words 8 through 15 to "freeze" the data in position. The most significant bit is restored as input to the DAC and the amplifier gain is readjusted to maintain the 5 volt full-scale indication, but now representing a ±5 volt data span for the input word. This channel, like the "Selected Word" channel, has an operational amplifier provided with zero adjust (R122) and full-scale adjust (R121) controls, and is provided with both an analog meter and a pair of jacks for an external digital voltmeter, as well as the galvanometer output amplitude adjustment.

3.10 Two additional digital-to-analog converters are provided within the unit and are hardwired to words 13 and 14, as described previously. These are also 8-bit DAC's and automatically provide adjustable analog output signals on the rear panel, proportional to the digital data available in words 13 and 14. If, in future applications, it proves desirable to monitor other words, it is a simple matter to re-connect the timing leads strobing these two latches, as wiring is quickly accessible by removing the top cover of the unit.

3.11 Overall operation of the "lock-loss" circuit has been described in general terms previously. Under normal data input conditions, IC107C serves as a "data present" detector. The output from the data conditioner, IC107A, is capacity coupled to one leg of exclusive or gate IC107C, with a positive DC return. Simultaneously, the same signal is inverted by IC106D and applied to the second input of the gate. So long as regular data is clocking through the data

conditioner, this exclusive or gate will always have opposite polarity signals on the two inputs, resulting in a "high" at output pin 10. Momentary transients (as transitions occur) are filtered out by capacitor C110, and output inverted by IC112C to a "low". This signal is then applied to or gate IC102A, and has no effect on the "lock-loss" driver. In the event there is no signal input, pin 3 of IC107A will go low and, as soon as C109 discharges, pin 8 of IC107C will be returned to the +5 volt line. The "low" signal input is inverted by IC106D and appears as a "high" signal on pin 9 of the data-loss detector. Since both signals are now "high", the output at pin 10 will go "low", be inverted by IC107C to a "high", gated through IC102A to lamp driver IC101F, and so will immediately illuminate the "lock-loss" light until signal is restored.

Under normal (synchronized) conditions of operation, with a frame sync word properly detected, only narrow reset spikes will occur at the "16" output at pin 5 of IC110. This very narrow pulse, coupled through or gate IC102B, is filtered out by C102, and thus no trigger is provided to multivibrator IC103B. In the event frame sync is not detected, pin 5 of IC110 will go high long enough to charge C102 and trigger the one-shot IC103B, which will then generate a pulse sufficiently wide to drive through or gate IC102A, and the lamp driver, IC101F, illuminating the "lock-loss" light. As soon as synchronization is restored, the width of the signal at pin 6 of or gate IC102B is too narrow to trigger the multivibrator and the lamp will go out again.

When in the subframe mode of operation, a similar philosophy is used with the "frame 8" output from pin 9 of the frame counter/decoder, IC121, taken through the "Normal/Housekeeping" switch to the pin 5 input of or gate IC102B. Under these conditions, lock loss multivibrator IC103B is again triggered, illuminating the "lock-loss" light. However, in this mode of operation, triggerring occurs at subframe rate, rather than frame rate, and the light may be observed to flicker.

3.12 To generate synthetic digital signals for internal calibration of the unit, the "Op/Cal" switch, S101, disconnects the data input line and provides, for input clocking to the data conditioner, a free-running square wave generated by IC106E and F. Frequency is determined by C103 and R102, and is approximately 15 KHz in this mode of operation. The clock signal is run through the data conditioner and provides a bit clock signal, through the remainder of the decoder. In the "0%" cal position, input to the shift register is grounded

by the arm of S101B and so the signal clocks a continuing sequence of 0's into the shift register, filling the entire register with 0's and insuring that the digital display for the selected word (and all downstream DAC's) will be at the "0" calibration point. When transferred to the "50%" cal mode, clock pulses from the cal oscillator are counted down by bit counter IC109 and used to trigger the word clock multivibrator, IC108D. This drives the remainder of the decoder, and also resets the most significant bit cal generator, IC111A. This type D flip-flop is then "set" by the leading edge of the word clock, and "reset" by the next following bit clock. The net effect is to generate a signal one bit wide at pin 2. The $\bar{Q}$ appears at the input to the shift register, is clocked in, and progresses through the register. Timing of the word clock pulse is such that all data latches will strobe this into position as the most significant bit, no matter which word is selected, resulting in a half-scale analog output from all DAC's and illumination of only the most significant bit in the digital display. Finally, in the "100%" cal position, the data input to the shift register is returned to the +5 volt line, and all 1's are clocked in, filling the register, so that all words receive full scale (all 1's) indication, insuring that all DAC's are driven to the maximum output.

It should be noted that the second section of the "Op/Cal" switch, S103B, is also provided with an "inverted data" position. Although "normal" data is normally taken from pin 3 of IC107A, this data is also available in inverted form from pin 9 of IC106D. If, for example, the data input is inverted, either through the use of an inverted sense discriminator in an FM/FM complex, or through use of an inverted data line from other sources, the data can be reinverted by proper choice of the position of this switch.

The input data stream for the "PCM Input" jack is also available at the "Data Monitor" BNC connector on the front panel.

3.13 For convenience in operating the decoder in conjunction with computer-controlled testing, a standard parallel output connector, S0101, has been provided on the rear panel. Undelayed 10-bit data from the data conditioner is fed as input to the "all words" data latch, IC126/127, which provides 10 parallel line output from the serial in/parallel out latch. Data is clocked through by the bit clock and strobed into position by the word clock at the end of each word, thus presenting a 10-line output, in parallel form, of the binary digital word, updated at the beginning of each word.

A "word address" generator, reset to 0 by the detected frame sync pulse

and then counting word lock pulses, also generates word addresses within chip IC128A and B. This chip is a ripple counter with BCD output; that is, 4 lines per digit in 1, 2, 4, 8 coding. IC128A serves to derive a 4-bit BCD coded "units" signal; "carry" to IC128B is used to generate the first two digits of a BCD "tens" code. (Note that, under normal conditions only the "one" line for the 10's will ever be energized, since there are only 16 words to the frame.) However, because of the frame sync inversion, it is possible that, under certain conditions of operation, one may obtain synchronization only on alternate frames, in which case the count could advance as far as 32. If this condition occurs, the associated computer will receive a word address greater than 16, and will so indicate. Normally, the reset line will clear this register back to 0 at the time of minor frame sync. The 6 lines corresponding to the 2 digit word address are taken though IC129, a hex flip-flop, where they are latched into place by the word clock signal, providing units and tens word addresses, in synchronism with the 10-line parallel data output.

3.14 Self-contained operation is provided by a provision of two power supplies within the unit. PS101 generates ±15 volt regulated power busses, balanced to ground, at a current capacity of 200 milliamperes each. PS102, also a commercial module, provides regulated +5 volts at a capacity of 250 milliamperes. Input power is fused by one-half amp fuse F101, and switched by S104 to turn the unit on and off; the LED "Power on" panel lamp is actuated by the output of the 5 volt power supply, through current limiting resistor R124, to provide and indication of the power "on" condition.

3.15 In addition of the normal PCM decoder functions, two auxiliary pieces of apparatus have been constructed within the same box, for convenience in field use. The first of these consists of a commercial line driver, IC201, which has both input and output connections brought out on BNC connectors on the rear panel. Input can be either direct coupled or through a blocking capacitor, by selection of the proper input connector jack. The input signal is provided with a gain control through R201 and used as input to a power amplifier, Burr-Brown model 3329/03. The output signal is taken through R202, an isolation resistor of 22 ohms, to an "Output" BNC connector, and also through a shunt resistor, R203, to ground to keep the output line from floating. This line is capable of driving a terminated 50 ohm cable.

The second auxiliary feature is provided by dual operational amplifier, IC202, a 747 chip. The two sections of this dual amplifier are wired in

cascade to provide a high gain audio amplifier. Input is by means of the standard microphone connector such as is normally used with the OSU voice equipment, and the output is taken across an adjustable output control, R212, to a BNC connector. This is of convenience when it is desired to provide voice modulation from a low level microphone to an associated tape recorder or amplifier.

The two above units are most frequently used as accessory equipment for adding audio tracks to an associated VCO multiplex, for tape recording. A power switch, S105, on the rear panel permits disconnecting the $\pm$15 volt busses, to de-energize circuitry when such use is not desired. For normal use, a low level microphone connected to JS107 can be used with the gain adjusted to the desired level to provide a 0 to 5 volt output signal, in order to drive an associated VCO in the multiplex system. In tape playbacks, the output of the associated discriminator can be taken through the line driver directly to a low impedance loud speaker, to provide an audible monitor of the playback. Since these two portions of the circuit are independently constructed and draw only power from the parent unit, they are for general utility for field support services.

4.0 PHYSICAL DESCRIPTION

The detailed drawing of the front and rear panel of the completed unit, which measures 3" high by 12" wide by 8" deep, is shown in OSU drawing C90TD14. The top panel is removeable by means of six screws. Immediately under the panel will be found a set of drawings and a complete set of operational spare parts for field operation, recessed into a foam plastic block. This block is so contoured as to hold all chips and components within the wirewrap board on which the major portion of the construction is accomplished. Details of the board layout and parts location will be found on OSU drawing C90TD13.

Although screw driver adjustment gain controls for the auxiliary line driver and audio microphone preamplifier will be found on the rear panel, all required operating controls are located on the front panel, for convenience. "Zero" and "full scale" adjustments for the operational amplifiers for both the "Selected Word," and the housekeeping "E" DAC will be found at the 0 and 5 volt ends of the edgewise analog meters on the front panel. The six hexadecimal switches (S103) permitting switching the DAC's to the desired word location will be found in the center of the panel; immediately beneath each section is

a multi-turn screw driver pot, adjusting amplitude for the associated 5 volt dc output to the level desired for galvanometer drive. Labelling for the digital display, analog meter, and hexadecimal switch for the "Selected Word" DAC is indicated by the panel marking; on the right hand side of the panel a similar set of markings is provided for use with the associated "E" channel. Note that, within this cluster of controls, there is also a toggle-switch S102 marked "Normal" and "Housekeeping", which serves to select the subcom mode of operation (for frame 0 through 7) and reestablish gain factors for the analog conversion to represent only the positive 0 to 5 volt portion of the data band when used in the "Housekeeping" mode. In the "Normal" mode, the same hexadecimal switch S103-6 may be used in positions 8 through 15 for mainframe words, and IC132E will return to the normal bipolar input data representation for output scale factor.

Because the associated automated test equipment used for temperature testing normally draws its operating power from the associated PCM decoder, and the power supply provided within this unit is insufficient to supply this added load, two banana jacks have been provided on the rear panel for connection to an external 5 volt power supply when automated testing is required.

The basic PCM encoder design incorporated provision for a subcommutated housekeeping word. This word is normally assigned to word 15, and (as described in the theory of operation in section 3.0) the "E" DAC switch is so wired as to permit positions 0 thru 7 to be used for this subcommutation mode. (Positions 8 thru 15 are available for mainframe words, thru the same "E" DAC.) Because many coders are now flown without the subcommutation feature, using word 15 as a clear channel main frame word, construction of the decoder has been so arranged as to permit a quick changeover, deleting the subcommutation feature of the decoder operation in the "E" DAC channel. Mechanical construction of the unit has been so arranged as to permit a simple conversion for this application:

(1) Main frame word 0 thru 7 selector lines, from the first 5 sections of the hexadecimal switch, have been connected to a 16-pin DIP socket and carried over to positions 0 thru 7 of the "E" switch. Normally these lines are opened, and positions 0 thru 7 are driven from the frame counter/decoder, IC121.

(2) In the event the subcommutation feature is not being utilized in the coder which is being tested, the normal mode of operation for the "E" DAC

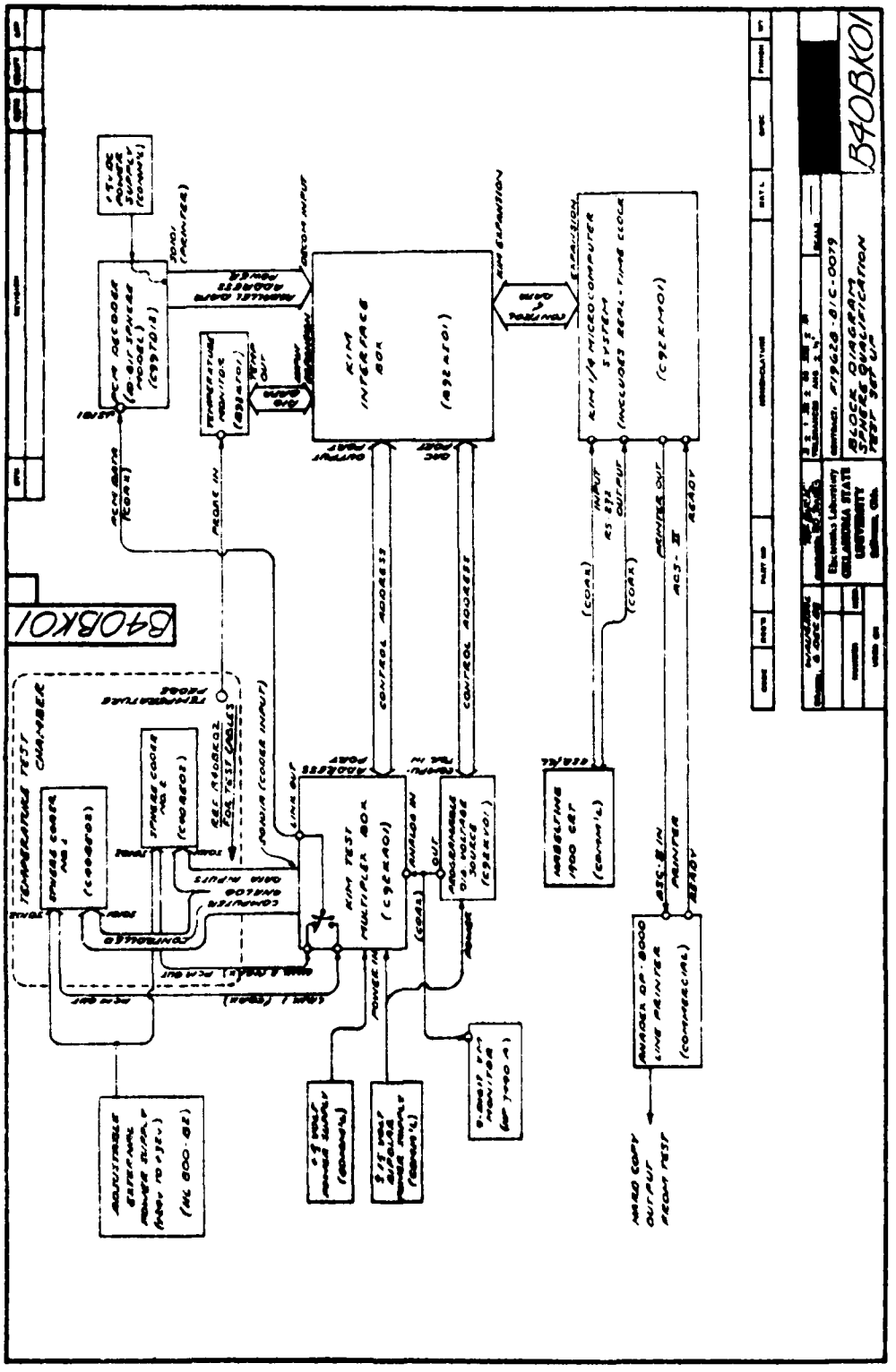

Figure 3. Block Diagram, Qualification Testing

selector switch can be restored by unplugging the CD4017BE chip from IC121. This chip should be removed and placed in the recess provided for this purpose in the foam hold-down block. At the same time, the plug-in jumper board should be inserted in the 16-pin DIP socket on the back of the hexadecimal switch. Jumper connections are such as to connect the hexadecimal switch to the normal lines for word 0 thru 15, thus permitting use of the "E" channel DAC for any desired word in the frame format.

5.0 QUALIFICATION TESTING OF SPHERE ENCODERS

Qualification testing is conducted with the equipment set up as shown in block diagram OSU drawing B40BK01 (Figure 3). The system in use is based upon the general procedure and methods, which were previously described in Scientific Report Number 1 under this contract (Reference 3). However, a number of changes have been made to update the automated test procedure, in order to incorporate modifications and additions to the set up, which have been incorporated since Reference 3 was written in August of 1981. Details of these additions and modifications are discussed in Appendices which follow this report.

5.1 Modifications to the automated test procedure incorporated for qualification testing of the sphere encoder may be summarized as including the following:

(a) Modification of the KIM interface box, D92KI02, in order to accept a word clock signal and detect frame synchronizing pulses from the associated OSU Model C90TD12 10-bit sphere decoder. (These changes were made because of the use of alternating frame synchronizing signals in the sphere encoder, and now permit use of the alternating frame sync detector of the decoder as a master synchronizing signal to the KIM system; the word clock is used to count words following each frame synchronizing signal.) The interface box has also been modified to incorporate the addition of the temperature sensor, (b) below, and the digital voltage reference generator, (c) below.

(b) Automatic sensing of the temperature within the test chamber has now been incorporated through use of the circuitry of OSU drawing B92KT01. The detected chamber temperature is automatically accepted by the KIM system, and is incorporated in the printout data.

(c) A programmable voltage reference generator, which permits computer program control for any designated analog reference voltage, has also been provided per OSU drawing C92KV01. The test routine permits programming a series of five test input voltages as desired for sphere testing, and these are also automatically controlled and printed out in the computer-controlled testing procedures.

(d) The KIM-1/4 system has also been modified now to incorporate a real-time clock card, per OSU drawing C99KM04. This clock permits automatic printout of the time at which each test run is begun, as a portion of the data printout from the testing procedure.

(e) The "breadboard" multiplex system of Reference 3, Figure 2, has now been replaced by a general purpose temperature test multiplexing system, as shown in OSU drawing C92KA01. This data multiplexing system, by means of the special sphere test cable, OSU drawing B41BK02, permits the KIM to automatically control tests of two Model C40BE02A 10-bit sphere encoders in a single qualification test run.

(f) A new set of computer programs have been developed for specific application to qualification testing of the 10-bit sphere encoder. Computer programs used for this purpose are as listed in Appendix A.

5.2 The outline of the qualification test procedure follows the general "manual set-up and checkout procedures," described originally in Reference 1. A considerably more elaborate and sophisticated test may now be conducted with the automated routines available through the computer-controlled system now in use. The test encompasses the following features:

(a) Each coder is tested at three separate input voltage supply values: (low voltage = 24 volts, nominal voltage = 28 volts, and high voltage = 32 volts, to the encoder under test). Each of these three voltages is used at each of three separate chamber temperatures in the course of the test routine. Temperatures used are: cold = $-20^{o}C$, normal = $+25^{o}C$, and hot = $+65^{o}C$.

(b) For each of the nine conditions of input supply voltage and temperature outlined above, the automated test system applies a set

of five selected input data voltages as analog signal input to mainframe words 1 through 13, and to subcommutated frames 1 through 7 of word 15, in a predetermined sequence. The five discrete voltages have been selected to give the desired 10-bit digital test words, as was described in Reference 1, Section 4.4.3. These were chosen to be near: just above the -5 volt lower limit, a -2.5 volt mid-range point, slightly above the 0 reference point, near the +2.5 volt mid-scale positive region, and just below the +5 volt upper limit.

(c) The test routine also uses the internal voltage monitor developed within the coder under test as data input to word 14, thus recording the digital (and analog equivalent values) of this housekeeping monitor through the PCM output of the encoder under test.

(d) For each condition and input voltage described above, the computer will take 1000 consecutive samples from each main frame word (or 100 consecutive samples from each subcommutated frame in word 15), and analyze the results noted.

(e) These samples are then sorted and a count is made of the number of occurrences of each digital code pattern which is detected through the auxiliary decoder.

(f) Each detected binary PCM code is then converted to the calculated analog test voltage which it represents.

(g) This calculated analog voltage is then compared to the actual input test voltage applied for the test, and the computer then calculates the error with respect to the input reference voltage.

(h) A hardcopy output is provided from all of the above tests, in order to document the full sequence of the qualification test.

5.3 A typical excerpt from the hard copy provided as printer output from the automated qualification test system is shown in Figure 4. This printout includes the following data:

(a) The date of the test and serial number of the Model C40BE02A encoder under test.

(b) The supply voltage to the coder and the temperature

SPHERE TEMPERATURE TEST 25 APRIL,83

ENCODER S/N? 9
LINK? 2
TIME 16 : 51 : 12 TEMPERATURE 23 C
POWER SUPPLY VOLTAGE? 28
INPUT VOLTAGE-4.9561

WORD#	BINARY VALUE	CALC VOLTAGE	ERROR	SAMPLES
1	00000001 00000000	-4.9561	0	1000
2	00000001 00000000	-4.9561	0	1000
3	00000001 00000000	-4.9561	0	1000
4	00000001 00000000	-4.9561	0	1000
5	00000001 00000000	-4.9561	0	1000
6	00000001 00000000	-4.9561	0	1000
7	00000001 00000000	-4.9561	0	1000
8	00000001 00000000	-4.9561	0	1000
9	00000001 00000000	-4.9561	0	1000
10	00000001 00000000	-4.9561	0	1000
11	00000001 00000000	-4.9561	0	1000
12	00000001 00000000	-4.9561	0	1000
13	00000001 00000000	-4.9561	0	1000
14	10100000 01000000	1.2646	6.22069	1000

********** SUBFRAME DATA **********

ENCODER S/N 9
WORD # 15
TIME 16 : 53 : 31 TEMPERATURE 23 C
INPUT VOLTAGE -4.9561
POWER SUPPLY VOLTAGE 28

FRM#	BINARY VALUE	CALC VOLTAGE	ERROR	SAMPLES
1	00000001 00000000	-4.9561	0	100
2	00000001 00000000	-4.9561	0	100
3	00000001 00000000	-4.9561	0	100
4	00000001 00000000	-4.9561	0	100
5	00000001 00000000	-4.9561	0	100
6	00000001 00000000	-4.9561	0	100
7	00000001 00000000	-4.9561	0	100

Figure 4. Sample Test Printout (Excerpt)

within the test chamber during the run which follows.

(c) The time at which the test is initiated.

(d) The analog input reference test voltage being applied for the run which follows.

(e) The run results are listed for each input voltage:

1. The identifying number of the word (or frame) being sampled.
2. Each binary PCM code pattern detected for this condition.
3. The calculated decimal input voltage indicated from this code.
4. The error of this calculated value with respect to the applied input reference voltage.
5. The number of occurrences of each of these code values within the total number of samples taken.

(f) The procedure will then repeat steps (b) through (e) above for the remaining sequence of four additional input analog test voltages, until the complete run of five test voltages has been completed.

(g) The automated test routine then stops, awaiting the operator to reset supply voltage and/or chamber test temperature to the desired value to initiate the next run.

(h) When placed back in the "run" mode at the desired temperature and voltage, it will repeat steps (a) through (g) again for the next run, until all nine runs of the qualification test have been completed for each coder under test.

(i) Since the test setup is capable of testing two coders at once, it will repeat the entire sequence for the second coder as well, when instructed by the operator that the second coder is now to be put in the test routine.

5.4 A detailed step-by-step procedure, which is to be followed to perform qualification tests, may be described as follows:

(a) Connect all equipment as shown in Figure 3, the block diagram, OSU drawing C40BK01. Coders under test should be within the temperature chamber, and the chamber will initially be at room temperature.

(b) Set the input supply voltage for the coders under test to the nominal 28 volt value.

(c) Initialize KIM system unit with the following step-by-step procedure:

1. Turn on Hazeltine keyboard.
2. Turn on KIM computer.

   Switch positions for computer

   A. 1 MHz
   B. Halt (Down)
   C. Normal
   D. Reset (Momentarily lift up)
   E. Printer interface set to inhibit

3. Hit return on keyboard

   A. Computer should respond with "KIM "
      FEE6 FF

4. Type in: D4ØØ
5. Hit space bar:

   A. Computer responds with D4ØØ D8

6. Hit "G" key
7. KIM responds with "LMON"
   "S"
8. Type in: MDCØØ,DCDØ,ØØØØ
9. Hit return
10. Hit return again (to get out of LMON mode)

    A. KIM responds with "D4ØØ D8"

11. Hit space bar

    A. KIM responds with "ØØØØ 20"

12. Hit "G" key
13. Put in Disk #1B (FODS)
14. KIM responds "FODS"
15. Type in: RUN %RTCSM
16. KIM responds:

    CLOCK ROUTINE
    INPUT (MO,DA,HR,MN,SC)CR

17. Type in the correct date and time. Example: ON DEC 12, @ 9:15:33 type in:

    12,12,09,15,33 then at the correct time, Hit return

    (Remember to use two digits per date. For example, the 9th hour: type in 09.)

18. KIM responds: "#"
19. Type in: RUN %BASP (Hit return)
20. KIM responds: Type in:

# of Lines/Page?	0 (Hit return)
Memory Size?	28600 (Hit return)
Terminal Width?	80 (Hit return)

21. Take out Disk #1B
22. Type in: Disk I (Hit return) (starts disk motor)
23. KIM responds: "21 STAT ERR","OK"
24. Put in Disk No. 17B (SPHERE,SPBA7)
25. Type in: DISKL,SPBA7 (Hit return)
26. KIM should respond with: "OK"
27. Type in: QUIT (Hit return)
28. KIM responds: "#"
29. Type in: "DIR" (Hit return) (Shows directory)
30. KIM responds with the directory,"#"
31. Type in: LOD %SPMCT
32. Hit "ESC" key and KIM responds: "ØØØØ 4C"
33. On computer front panel do the following:
    A. Move HALT to up position
    B. 2 MHz
    C. Move HALT to down position
    D. Hit RESET
34. Hit return key on keyboard
35. KIM responds with "ØØØØ 4C"
36. Type in: 17F2 (Space bar)
37. KIM should respond 17F2 ØB
38. If KIM responds 17F2 ØA then type in: ØB. (Make sure you type a period after ØB). This enters ØB into location 17F2 to set the baud rate between CRT and computer.
39. Hit the Space Bar
40. Hit "G" key
41. KIM should respond "OK."
42. Switch programmable voltage reference generator to "SWITCHES" mode and set switches on side to pattern of 1000 0000 0100 0000. (Monitor meter should read output voltage of +0.0244 volts.)
43. Type in: POKE 2048,00
    (This sets multiplexer to "Word 1" position, applying the test voltage to Word 1 of encoder under test.)

44. Using "Selected Word" DAC switch on sphere decoder, dial up Word 1 and check digital word display. Lamps should be illuminated for bits one and nine only. (All other words and frames will have open circuit inputs during this test.)

45. Set printer interface switch to "HANDSHAKE"

46. Type in: RUN (Hit return to start program)

47.

KIM responds:	Type in:
ENCODER S/N?	S/N of coder to be tested
LINK?	1 (for first coder; use 2 if switching to second unit in chamber)
POWER SUPPLY VOLTAGE?	Voltage being used (e.g., 28)

48. KIM will now make complete test run and tabulate results on printer, signifying completion by printing OK at lower right and stopping.

49. Reset power supply voltage (and/or temperature) to values desired for next run. When conditions are as desired:

50. Type in: RUN (Hit return key to start program)

51. Repeat steps 47 through 50 until tests have been completed for all required values for power supply voltage and chamber temperature (total of nine runs) for each coder under test.

LIST OF REFERENCES

1. Buck, Richard F.: Ten-Bit Resolution PCM Encoder. (Scientific Report No. 2 to F19628-78-C-0033). Electronics Laboratory-D.E.T.A., Oklahoma State University, Stillwater, Oklahoma (AFGL-TR-80-0071; February, 1980). AD A092111

2. Buck, Richard F.: Development of Instrumentation for Research Probes. (Final Report to F19628-78-C-0033). Electronics Laboratory-D.E.T.A., Oklahoma State University, Stillwater, Oklahoma. (AFGL-TR-81-0203; July, 1981). AD A107280

3. Spears, J.W.: Automated PCM Encoder Temperature Test. (Scientific Report No. 1 to F19628-81-C-0079). Electronics Laboratory-D.E.T.A., Oklahoma State University, Stillwater, Oklahoma. (AFGL-TR-81-0242; August, 1981). AD A108184

APPENDIX A

SOFTWARE LISTINGS

(All are on KIM Disk No. 17B; BASIC program revised on 22 November 1982 controls test, and invokes assembled machine code programs as subroutines.)

	Purpose	Program
A1	BASIC (Defines Qualification Test Routine for C40BE02 10-Bit Encoders)	SPBA7
A2	ASSEMBLED MACHINE CODE (Total assembled set of the sub-routines required.) Includes:	SPMCT
A2.1	SPHERE Main Frame Data (Subroutine to look at Main Frame Data, from Words 1-14)	SP-A
A2.2	SPHERE Subcom Data (Subroutine to look at Word 15 Subcommuted Data)	SP-AS
A2.3	Temperature and Clock Routine (Subroutine to convert the Temperature Data to Digital Form, and obtain Real Time clock data from computer)	TSCLA

```
LIST 1 GOTO 15  :REM TO CAL. USE (INPUT "1ST 8",A)
 2 INPUT "2ND 8";B
 3 POKE 4096,A
 4 POKE 4097,B
 5 GOTO 1
 15 REM   SPHERE.....SPHERE ENCODER TEMPERATURE TEST
 16 REM
 20 REM   THIS PROGRAM TAKES 1000 SAMPLES OF EACH MAINFRAME WORD
 21 REM   AND 100 SAMPLES OF EACH SUBCOM WORD. WORDS 1 THRU 14
 22 REM   ARE SAMPLED FIRST THEN THE SUBFRAME WORDS.
 23 REM   THIS ROUTINE CALLS THE MACHINE CODE PROGRAM "SPMC"
 24 REM   TO OBTAIN MAINFRAME AND SUBFRAME DATA.
 25 REM
 26 VR=0   :REM THERE ARE FIVE VR (VOLTAGE RUNS)
 28 PRINT
 29 DT$="22 NOVEMBER,82"
 30 PRINT TAB(22);"SPHERE TEMPERATURE TEST  ";DT$
 35 PRINT : PRINT:
 40 PRINT
 43 REM .....INITIALIZE ARRAY N FOR SUBFRAME DATA.....
 45 DIM N(25),V1(20)
 46 REM                    WORDS WILL BE PRINTED.
 47 FOR I=0 TO 7
 48 READ N(I)
 50 NEXT I
 51 FOR I=0 TO 18
 52 READ V1(I)
 53 NEXT I
 55 GOSUB 2000 : REM .....GET DATA FROM OPERATOR.....
 56 ST=1 : ED=14
 58 REM                ....INITIALIZE STARTING ADDR FOR ZIPMC
 59 REM                    THIS WILL READ MAINFRAME DATA
 60 POKE 8256,0
 65 POKE 8257,230
 70 REM               .....BEGIN LOOP FOR MAINFRAME DATA.....
 71 FOR A=ST TO ED
 72 POKE 2048,DL
 73 DL=DL+1
 80 HX=INT(A/10)
 90 WA=A-(HX*10)
 100 HX=HX*16+WA
 110 POKE 58920,HX
 111 GOSUB 119
 112 PRINT : NEXT A
 115 GOTO 380
 117 REM ...SUBROUTINE TO CALL MACHINE CODE PROGRAM
 118 REM            AND PRINT RESULTS. (STATEMENTS 119-340)
 119 J=0
```

```
120 X1=USR(J)
130 M=61376
140 SM=PEEK(M+2)
153 SP=PEEK(M+3)
155 IF SP+SM=0 THEN RETURN
160 FL=0
170 B$=""
190 DA=PEEK(M)
195 X=128
200 IF X<=DA THEN 230
210 B$=B$+"0"
220 GOTO 240
230 B$=B$+"1"
235 DA=DA-X
240 X=X/2
250 IF X>.5 THEN GOTO 200
260 DA=PEEK(M+1)
270 FL=FL+1
275 B$=B$+" "
280 IF FL=1 THEN GOTO 195
290 D1=PEEK(M)
300 D2=PEEK(M+1)
305 V=(D1+D2/256)/25.6
306 V=V+.00488    :REM DATA IS OFF BY 1/2 BIT.
311 VO=V
312 SM=(SP*256)+SM
313 V=INT((VO-5)*10000)/10000
315 VD=V-VI
316 VD=INT(VD*100000)/100000
320 PRINT TS$;A;TAB(12);B$;TAB(34);V;TAB(50);VD;TAB(66);SM
330 M=M+4
340 GOTO 140
345 REM
350 REM      ....ROUTINE TO OBTAIN AND PRINT SUBCOM DATA....
355 REM
380 PRINT
390 DL=DL+3
400 PRINT
402 PRINT TS$;"*************  SUBFRAME DATA  *************"
405 WD=15
410 ST=1 :ED=7
415 PRINT  PRINT
430 PRINT TS$;"ENCODER S/N";SM
435 PRINT TS$;"WORD # ";WD
436 GOSUB 2200
437 PRINT TS$+"INPUT VOLTAGE ";VI
438 PRINT TS$+"POWER SUPPLY VOLTAGE";PS
440 PRINT
```

```
450 R$="FRM#     BINARY VALUE        CALC VOLTAGE        ERROR
460 PRINT TS$+R$+TI$
470 POKE 8256,0
480 POKE 8257,231
525 FOR K=ST TO ED
530 FR=N(K)
535 PRINT
540 POKE 2048,DL
545 DL=DL+1
550 HX=INT(FR/10)
555 WA=FR-(HX*10)
560 HX=HX*16+WA
570 POKE 59226,HX
575 A=FR
580 GOSUB 119
590 NEXT K
600 IF VR>8 THEN END
610 PRINT:PRINT:PRINT
620 GOTO 55
900 REM
910 REM      .....LIST OF SUBFRAME WORDS.  FIRST DATA
1000 DATA 0,1,2,3,4,5,6,7
1010 DATA 64,135,95,112,128,75,160,150,191,130
1020 DATA -4.9561,0,-2.5440,0,.0244,0,2.5439,0,4.9560
1030 REM SET TO: -4.9560,-2.546,.023,2.546,4.958
1890 REM
1900 REM      ....SUBROUTINE TO OBTAIN LINK,TEMPERATURE, &
1910 REM           INPUT VOLTAGE FROM OPERATOR AND TO
1920 REM           PRINT DATA HEADING.
1930 REM
2000 TI$="     SAMPLES"
2003 IF VR>0 THEN 2027
2005 PRINT
2007 INPUT "     ENCODER S/N";SN
2009 INPUT "     LINK";LI
2010 GOSUB 2200    :REM GET TIME AND TEMPERATURE
2020 INPUT "     POWER SUPPLY VOLTAGE";PS
2025 GOSUB 2500
2026 GOTO 2035   :REM DO NOT PRINT
2027 PRINT TS$;"ENCODER S/N";SN
2030 GOSUB 2200    :REM GET TIME AND TEMPERATURE
2031 PRINT TS$+"POWER SUPPLY VOLTAGE";PS
2032 GOSUB 2500
2035 TS$="          "
2040 T$="WORD#    BINARY VALUE        CALC VOLTAGE        ERROR
2050 PRINT
2060 PRINT TS$+T$+TI$
2070 PRINT
```

```
2075 REM      ....INITIALIZE DL (THE OUTPUT PORT VARIABLE)
2085 IF LI=2 THEN DL=24
2090 IF LI=1 THEN DL=0
2100 RETURN
2190 REM
2195 REM
2200 REM   TEMPERATURE ROUTINE
2210 POKE 8256,00
2220 POKE 8257,232     :REM $E800
2230 J=0
2240 X=USR(J)
2250 U1=PEEK(768)    :REM GET UPPER BYTE $0300
2260 U2=PEEK(769)    :REM GET LOWER BYTE
2270 VP=((U1*4)+U2)*.00488
2280 VP=INT((.005+VP)*100)
2290 TP=(VP-273)     :REM 0C=2.7315V
2300 POKE 8256,80     :REM $E850
2310 POKE 8257,232
2320 J=0
2330 X=USR(J)
2340 T=59538          :REM $E892
2350 S=PEEK(T)
2360 M=PEEK(T+1)
2370 H=PEEK(T+2)
2375 CE$="      TIME"
2376 CF$="              TEMPERATURE"
2380 PRINT CE$;H;":";M;":"S;CF$;TP;"C"
2390 RETURN
2500 REM VOLTAGE ROUTINE
2520 POKE 4096,VI(VR)
2530 POKE 4097,VI(VR+1)
2540 VI=VI(VR+10)
2560 PRINT "      INPUT VOLTAGE";VI
2570 VR=VR+2
2580 RETURN
OK
```

```
 10 0000           ; SPHERE.....FOR MAIN FRAME DATA
 20 0000           ; SP-A
 30 0000           ; 10/1/82
 40 0000           ;
 50 0000           ; SPMC IS THE MACHINE CODE FORM OF THIS PROGRAM.
 60 0000           ;
 70 0000           ;
 80 0000           ; SUBROUTINE TO BE USED IN CONJUNCTION WITH BASIC
 90 0000           ; TO LOOK AT DATA FROM THE DECOM....USE WITH SPBA7
100 0000           ;
110 0000           ; THIS ROUTINE SAMPLES A WORD 1000 TIMES AND
120 0000           ; COUNTS THE # OF WORDS THAT ARE A LIKE.  THERE
130 0000           ; ARE ONLY 8 DIFFERENT BIT PATTERNS RETAINED.
140 0000           LOC0=$EFB0
141 0000           LOC1=LOC0+1
142 0000           LOC2=LOC0+2
143 0000           LOC3=LOC0+3
144 0000           LOCF=LOC0+15
150 E600           *=$E600
160 E600           TABLE =LOC0+16
170 E600                                    ;
180 E600 A240      ZIPA    LDX #$40         ; ZERO THE TABLE
190 E602 A900              LDA #0
200 E604 9DBFEF    LOOPA   STA LOCF,X
210 E607 CA                DEX
220 E608 D0FA              BNE LOOPA
230 E60A A000              LDY #0
240 E60C 8CB0EF            STY LOC0         ; TOTAL SAMPLES=0
250 E60F A903              LDA #$03         ;SET HI BYTE OF # OF SAMPLES
260 E611 8DB3EF            STA LOC3
270 E614 A9EB              LDA #$EB         ;SET LOW BYTE OF # OF SAMPLES
280 E616 8DB2EF            STA LOC2
290 E619 ADB2EF    TSAM    LDA LOC2         ; GET # OF SAMPLES
300 E61C CDB0EF            CMP LOC0
310 E61F F068              BEQ CKSAM
320 E621 C020      NOISE   CPY #$20         ; IF=20 THEN "ITS REAL NOISY!!"
330 E623 F069              BEQ END
340 E625 A200      TABPT   LDX #$00         ; SET TABLE POINTER=0
350 E627 A900              LDA #$00         ; GET WORD # FROM BASIC
360 E629 2C0304    WDCLK   BIT $403         ; IS WORDD CLOCK HI?
370 E62C 10FB              BPL WDCLK
375 E62E EA                NOP              ;DELAY
376 E62F EA                NOP
380 E630 CD0004    LOOPB   CMP $400         ; GET WORD ADDRESS
390 E633 D0F4              BNE WDCLK
400 E635 EEB0EF            INC LOC0         ; INC THE TOTAL SAMPLES
410 E638 C000              CPY #00          ; IS THIS FIRST SAMPLE
420 E63A D01E              BNE NEWDAT
430 E63C AD0104    GETHI   LDA $401         ; GET HI DATA (MSB'S)
440 E63F 9DC0EF            STA TABLE,X      ; PUT INTO TABLE
450 E642 E8                INX
460 E643 AD0204            LDA $402         ; GET LOW DATA
```

```
470 E646 9DC0EF          STA TABLE,X
480 E649 E8              INX
490 E64A FEC0EF          INC TABLE,X ; INC# SAMPLES FOR THIS DATA
500 E64D D005            BNE XPLUS   ; IF LO CNT=0 THEN INC
510 E64F E8              INX
520 E650 FEC0EF          INC TABLE,X ; INC HI CNT
530 E653 CA              DEX
540 E654 E8       XPLUS  INX
550 E655 E8              INX
560 E656 8A              TXA         ; SET Y=X
570 E657 A8              TAY
580 E658 10BF            BPL TSAM    ; GO CHECK TOTAL SAMPLES
590 E65A AD0104   NEWDAT LDA $401    ; GET HI DATA
600 E65D DDC0EF          CMP TABLE,X ; = TO TABLE VALUE?
610 E660 F00E            BEQ TESTLO
620 E662 E8       SETX3  INX         ; X=X+4
630 E663 E8       SETX2  INX
640 E664 E8              INX
650 E665 E8              INX
660 E666 8EB1EF          STX LOC1    ; SAVE X TO CMP
670 E669 CCB1EF          CPY LOC1    ; DOES X=Y??
680 E66C D0EC            BNE NEWDAT  ; GO GET NEXT TABLE VALUE
690 E66E F0CC            BEQ GETHI   ; GO PUT INTO TABLE
700 E670 E8       TESTLO INX
710 E671 AD0204          LDA $402    ; GET LOW DATA
720 E674 DDC0EF          CMP TABLE,X ; = TO TABLE VALUE?
730 E677 D0EA            BNE SETX2
740 E679 E8              INX
750 E67A FEC0EF          INC TABLE,X ; INC THE SAMPLE CNT
760 E67D F003            BEQ HISAM   ; IF=0 THEN INC HI SAMPLE CNT
770 E67F 4C19E6          JMP TSAM
780 E682 E8       HISAM  INX
790 E683 FEC0EF          INC TABLE,X ; INC HI SAM CNT
800 E686 4C19E6          JMP TSAM
810 E689 CEB3EF   CKSAM  DEC LOC3    ; DEC HI SAMPLE CNT
820 E68C 1001            BPL SETLO
830 E68E 60       END    RTS
840 E68F A9FF     SETLO  LDA #$FF     ; SET LO CNT
850 E691 8D82EF          STA LOC2
860 E694 A900            LDA #$00    ; RESET CNT
870 E696 8D80EF          STA LOC0
880 E699 4C19E6          JMP TSAM


MEMORY USED: 31FE-3AC9

KIM
F300 4C G
```

```
 10 0000           ; SPHERE.....FOR SUBCOM USE
 20 0000           ; 10/1/82
 30 0000           ;
 40 0000           ; SUBROUTINE TO BE USED IN CONJUNCTION WITH BASIC
 50 0000           ; TO LOOK AT DATA USE SPHERE DECODER
 60 0000           ;
 70 0000           ; THIS ROUTINE SAMPLES A SUBCOM WORD 100 TIMES AND
 80 0000           ; COUNTS THE # OF WORDS THAT ARE A LIKE.  THERE
 90 0000           ; ARE ONLY 8 DIFFERENT BIT PATTERNS RETAINED.
100 0000           LOC0 =$EFB0
101 0000           LOC1=LOC0+1
102 0000           LOC2=LOC0+2
103 0000           LOC3=LOC0+3
104 0000           LOC4=LOC0+4
105 0000           LOCF=LOC0+15
110 E700           *=$E700
120 E700           TABLE =LOC0+16
130 E700                                    ;
140 E700 A240      ZIPA    LDX #$40         ; ZERO THE TABLE
150 E702 A900              LDA #0
160 E704 9DBFEF    LOOPA   STA LOCF,X
170 E707 CA                DEX
180 E708 D0FA              BNE LOOPA
190 E70A A000              LDY #0
200 E70C 8CB0EF            STY LOC0
210 E70F A900              LDA #$00
220 E711 8DB3EF            STA LOC3
230 E714 A964              LDA #$64         ; SET SAMPLES=100
240 E716 8DB2EF            STA LOC2
250 E719 ADB2EF    TSAM    LDA LOC2         ; GET # OF SAMPLES
260 E71C CDB0EF            CMP LOC0
270 E71F D003              BNE NOISE
280 E721 4CBFE7            JMP CKSAM
290 E724 C020      NOISE   CPY #$20         ; IF=20 THEN "ITS REAL NOISY!!"
300 E726 D003              BNE TABPT
310 E728 4CC4E7            JMP END
320 E72B A200      TABPT   LDX #$00         ; SET TABLE POINTER=0
330 E72D A915      LOOP1   LDA #$15         ;WORD 15
335 E72F EA                NOP
336 E730 EA                NOP
340 E731 2C0304    WDCLK   BIT $403         ; IS WORDD CLOCK HI?
350 E734 10FB              BPL WDCLK
```

```
360 E736 CD0004          CMP $400     ; GET WORDD ADDRESS
370 E739 D0F6            BNE WDCLK
380 E73B AD0104          LDA $401     ; GET HI DATA
390 E73E C900            CMP #00      ; TEST FOR ALL ZEREOS
395 E740 D0EB            BNE LOOP1    ; (FR 0,WD 15 IS ALL ZERO'S)
400 E742 AD0204          LDA $402     ; GET LO DATA
405 E745 C900            CMP #00
410 E747 D0E4            BNE LOOP1
412 E749           ;
413 E749           ; FOUND FRAME 0 ,NOW LOOK FOR DESIRED FRAME.
415 E749 A900            LDA #00
420 E74B 8DB4EF          STA LOC4
425 E74E 2C0304    FRCLK BIT $403
430 E751 50FB            BVC FRCLK
440 E753 EEB4EF          INC LOC4
445 E756 ADB4EF          LDA LOC4
450 E759 C900            CMP #00      ;CMP WITH DESIRED FRAME# (FROM BASIC)
460 E75B D0F1            BNE FRCLK
470 E75D A915            LDA #$15     ;WORD 15
471 E75F 2C0304    WDCLK1 BIT $403     ; IS WORD CLK HI?
472 E762 10FB            BPL WDCLK1
475 E764 EA              NOP
476 E765 EA              NOP
480 E766 CD0004          CMP $400     ; GET WORD ADDRESS
490 E769 D0F4            BNE WDCLK1
500 E76B EEB0EF          INC LOC0
510 E76E C000            CPY #0       ; IS THIS FIRST SAMPLE?
520 E770 D01E            BNE NEWDAT
530 E772 AD0104    GETHI LDA $401     ; GET HI DATA
540 E775 9DC0EF          STA TABLE,X ; PUT INTO TABLE
550 E778 E8              INX
560 E779 AD0204          LDA $402     ; GET LOW DATA
570 E77C 9DC0EF          STA TABLE,X
580 E77F E8              INX
590 E780 FEC0EF          INC TABLE,X ; INC# SAMPLES FOR THIS DATA
600 E783 D005            BNE XPLUS   ; IF LO CNT=0 THEN INC HI CNT
610 E785 E8              INX
620 E786 FEC0EF          INC TABLE,X ; INC HI CNT
630 E789 CA              DEX
640 E78A E8        XPLUS INX
650 E78B E8              INX
660 E78C 8A              TXA         ; SET Y=X
670 E78D A8              TAY
```

```
680 E78E 1089          BPL TSAM     ; GO CHECK TOTAL SAMPLES
690 E790 AD0104 NEWDAT LDA $401     ; GET HI DATA
700 E793 DDC0EF        CMP TABLE,X  ; = TO TABLE VALUE?
710 E796 F00E          BEQ TESTLO
720 E798 E8     SETX3  INX          ; X=X+4
730 E799 E8     SETX2  INX
740 E79A E8            INX
750 E79B E8            INX
760 E79C 8EB1EF        STX LOC1     ; SAVE X TO CMP
770 E79F CCB1EF        CPY LOC1     ; DOES X=Y??
780 E7A2 D0EC          BNE NEWDAT   ; GO GET NEXT TABLE VALUE
790 E7A4 F0CC          BEQ GETH1    ; GO PUT INTO TABLE
800 E7A6 E8     TESTLO INX
810 E7A7 AD0204        LDA $402     ; GET LOW DATA
820 E7AA DDC0EF        CMP TABLE,X  ; = TO TABLE VALUE?
830 E7AD D0EA          BNE SETX2
840 E7AF E8            INX
850 E7B0 FEC0EF        INC TABLE,X  ; INC THE SAMPLE CNT
860 E7B3 F003          BEQ HISAM    ; IF=0 THEN INC HI SAMPLE CNT
870 E7B5 4C19E7        JMP TSAM
880 E7B8 E8     HISAM  INX
890 E7B9 FEC0EF        INC TABLE,X  ; INC HI SAM CNT
900 E7BC 4C19E7        JMP TSAM
910 E7BF CEB3EF CKSAM  DEC LOC3    ; DEC HI SAMPLE CNT
920 E7C2 1001          BPL SETLO
930 E7C4 60     END    RTS
940 E7C5 A9FF   SETLO  LDA #$FF     ; SET LO CNT
950 E7C7 8DB2EF        STA LOC2
960 E7CA A900          LDA #$00     ; RESET CNT
970 E7CC 8DB0EF        STA LOC0
980 E7CF 4C19E7        JMP TSAM
```

```
MEMORY USED: 31FE-3C29

KIM
F300 4C G
```

```
 10 0000           ;            TEMPERATURE CONVERSION ROUTINE
 11 0000           ;             AND REAL TIME CLOCK ROUTINE
 12 0000           ;
 15 0000           ;11/18/82
 16 0000           ;
 18 0000           ; TSCLA (TEMPERATURE SENSOR AND CLOCK ASSEMBLY)
 20 E800           *=$E800
 30 E800           LBYTE=$0301
 40 E800           UBYTE=$0300
 50 E800           ;
 60 E800           ;
 70 E800           ; INPUT ROUTINE TO CONVERT TEMP. TO DIGITAL
 80 E800 A920      BEGIN   LDA #$20
 90 E802 8D0008            STA $0800        ;TRIGGER IN (HIGH)
100 E805 A905              LDA #05          ;TRIGGER PW>1MICRO SECOND
110 E807 8D0417            STA $1704
120 E80A 2C0517   DELAY    BIT $1705        ; /1 MICROSECOND
130 E80D 10FB              BPL DELAY        ;WAIT 5 MICROSECONDS
140 E80F          ;
150 E80F A900              LDA #00           ;TRIGGERS ON NEG.EDGE
160 E811 8D0008            STA $0800
170 E814          ;
180 E814 A20A              LDX #10           ;TEST FOR EOC. PULSE
190 E816 CA       HERE     DEX
200 E817 F0E7              BEQ BEGIN
210 E819 2C010C            BIT $C01
220 E81C 10F8              BPL HERE
230 E81E 2C010C   HERE1    BIT $C01           ;RETURN WHEN EOC COMPLETE.
240 E821 30FB              BMI HERE1
250 E823 AD010C            LDA $C01
260 E826 2930              AND #$30
270 E828 4A                LSR A
280 E829 4A                LSR A
290 E82A 4A                LSR A
300 E82B 4A                LSR A
310 E82C 8D0103            STA LBYTE
320 E82F AD000C            LDA $C00
330 E832 8D0003            STA UBYTE
340 E835 60                RTS
350 E836          ;
```

```
400 E836            ; RE AL TIME CLOCK ROUTINE
410 E836            ;
420 E836                    ;$0D07    $E897  MONTH
430 E836                    ;$0D06    $E896  DAY OF MONTH
440 E836                    ;$0D05    $E895  DAY OF WEEK
450 E836                    ;$0D04    $E894  HOURS
460 E836                    ;$0D03    $E893  MINUTES
470 E836                    ;$0D02    $E892  SECONDS
480 E836                    ;$0D01    $E891  HUNDREDS AND TENTHS
490 E836                    ;$0D00    $E890  TEN THOUSANDS OF SEC
500 E836            ;
510 E836                  TABLE=$E890
520 E850                  *=$E850   ;MUST BE AT ADDR.W/AB4 HIGH
530 E850 A207             LDX #$07
540 E852 BD000D   AGAIN   LDA $0D00,X
550 E855 AD400D           LDA $0D40
560 E858 9D90E8           STA TABLE,X
570 E85B 2062E8           JSR HEX    ;CONVERT BCD TO HEX
580 E85E CA               DEX
590 E85F D0F1             BNE AGAIN
600 E861 60               RTS
610 E862            ;
620 E862 4A         HEX   LSR A
630 E863 4A               LSR A
640 E864 4A               LSR A
650 E865 4A               LSR A
660 E866 A8               TAY
670 E867 F008             BEQ HERE2
680 E869 18               CLC
690 E86A A900             LDA #00
700 E86C 6906       ADD   ADC #$06
710 E86E 88               DEY
720 E86F D0FB             BNE ADD
730 E871 8D79E8   HERE2   STA SUB+1
740 E874 BD90E8           LDA TABLE,X
750 E877 38               SEC
760 E878 E900       SUB   SBC #00
770 E87A 9D90E8           STA TABLE,X
780 E87D 60               RTS
```

MEMORY USED: 31FE-379F

KIM
F300 4C G